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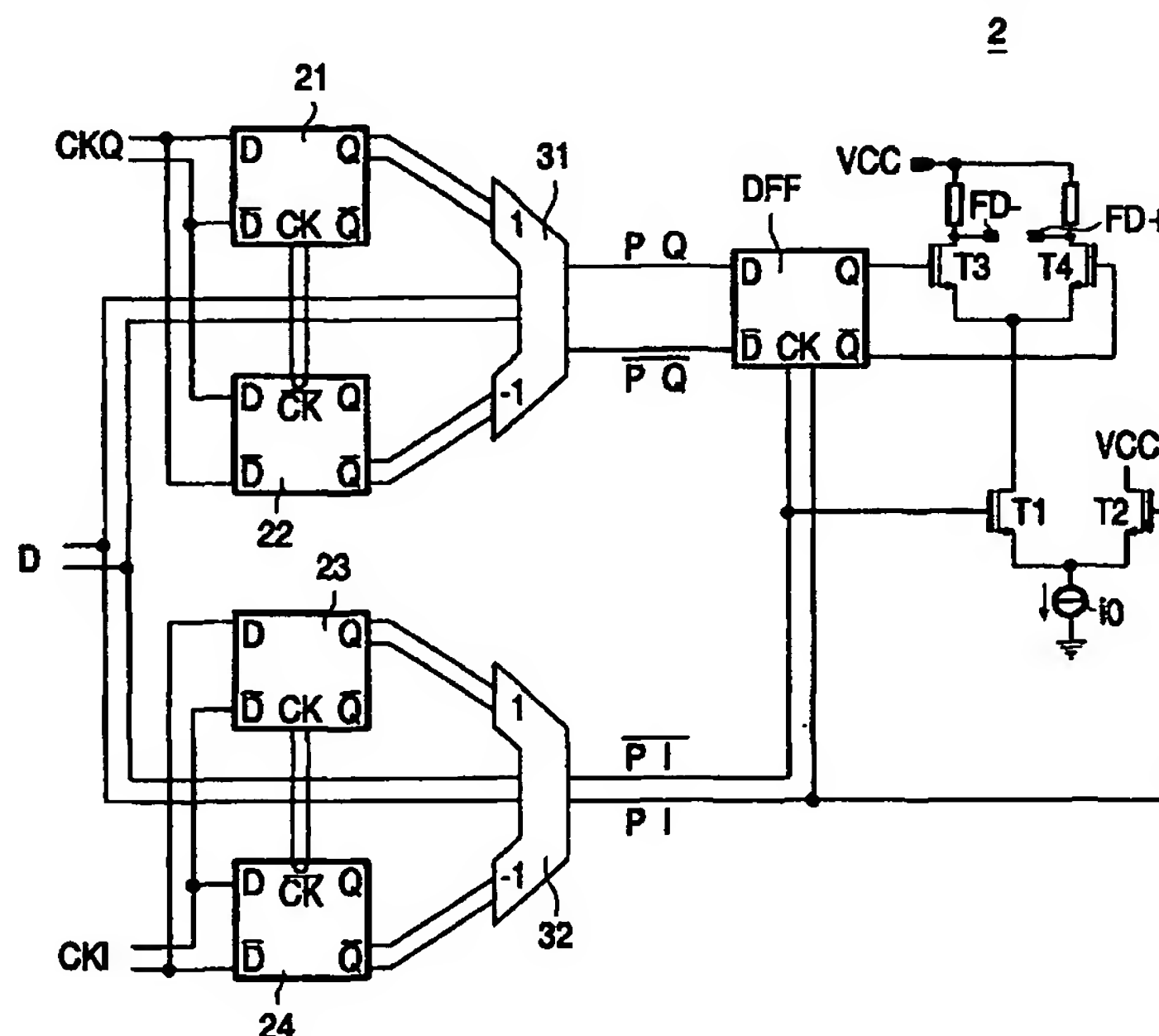
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(54) Title: PLL USING UNBALANCED QUADRICORRELATOR



(57) Abstract: A Phase Locked Loop (1) used in a data and clock recovery comprising a frequency detector (10) including a quadri-correlator (2), the quadricorrelator (2) comprising a frequency detector including double edge clocked bi-stable circuits (21, 22, 23, 24) coupled to a first multiplexer (31) and to a second multiplexer (32) being controlled by a signal having a same bitrate as the incoming signal (D), and a phase detector (DFF) controlled by a first signal pair (PQ, P \overline{Q}) provided by the first multiplexer (31) and by a second signal pair (PI, P \overline{I}) provided by the second multiplexer (32).

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